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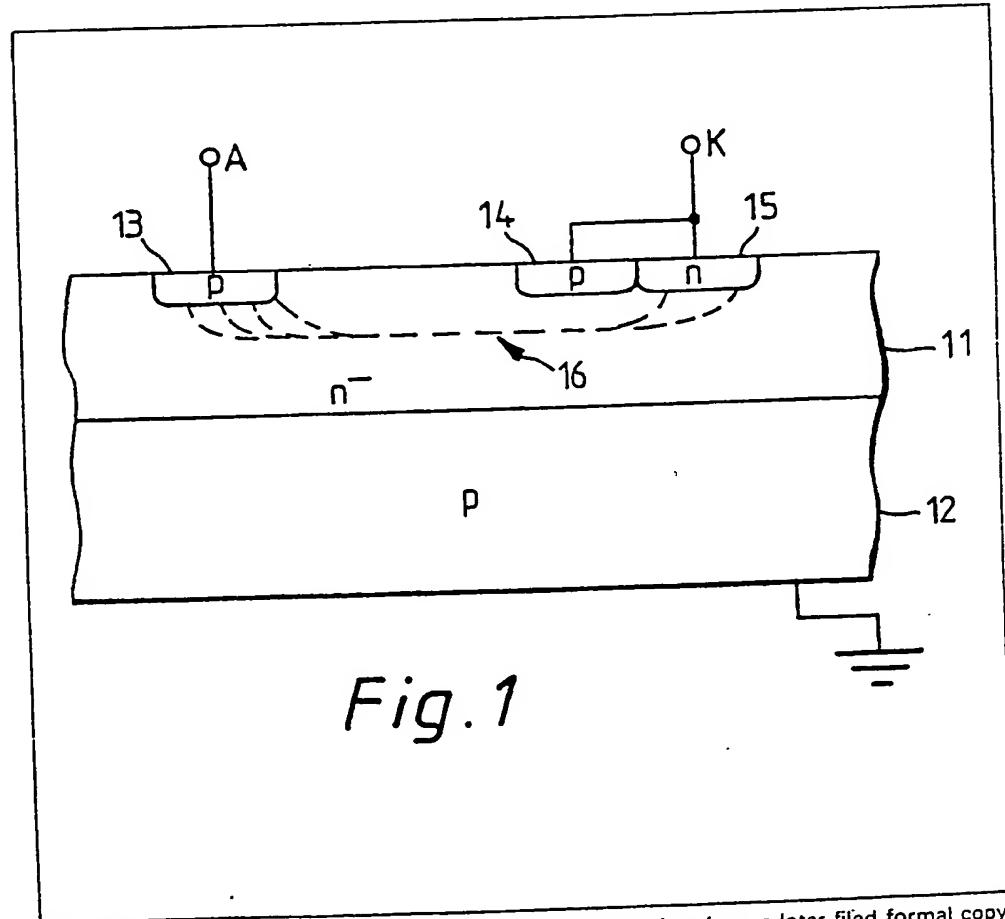
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(54) Semiconductor protection de-
vice for integrated circuits

(57) A breakdown protection device
for a bipolar integrated circuit com-
prises spaced p type regions (13,
14) disposed in an n-type epitaxial
layer (11) on a p-type substrate
(12). An n-type diffusion (15) is
faced adjacent the p-type region
(14), these two regions being con-
nected together to form the cathode
terminal of the arrangement. The
other p type diffusion (13) forms
the anode and together with the
substrate is normally earthed. Pas-
sage of a breakdown current in-
duces both lateral and vertical tran-
sistor action to provide a low impe-
dence breakdown path. Avalanche
breakdown occurs across the junc-
tion between region 13 and the
layer 11.



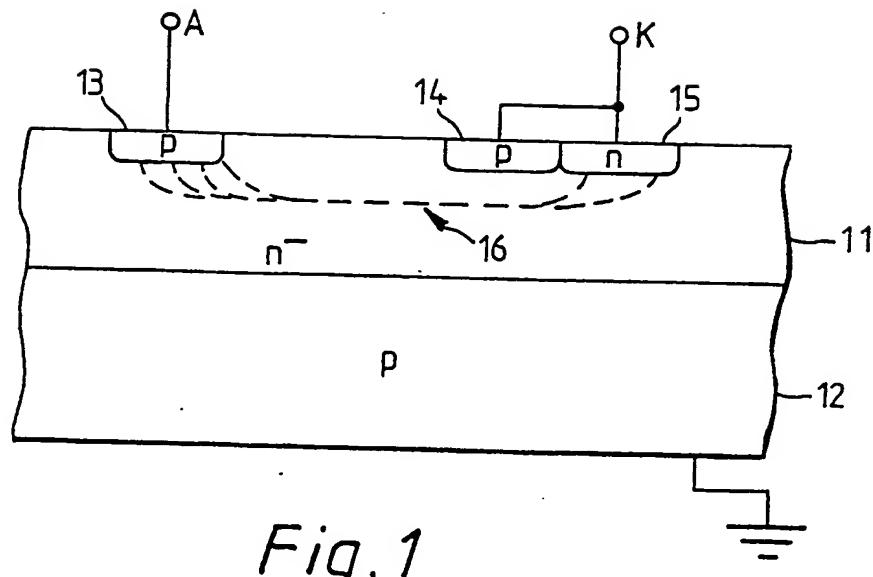


Fig. 1

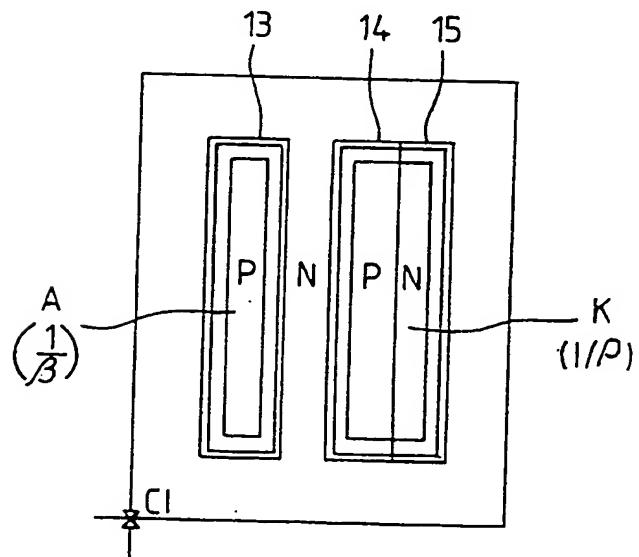


Fig. 2

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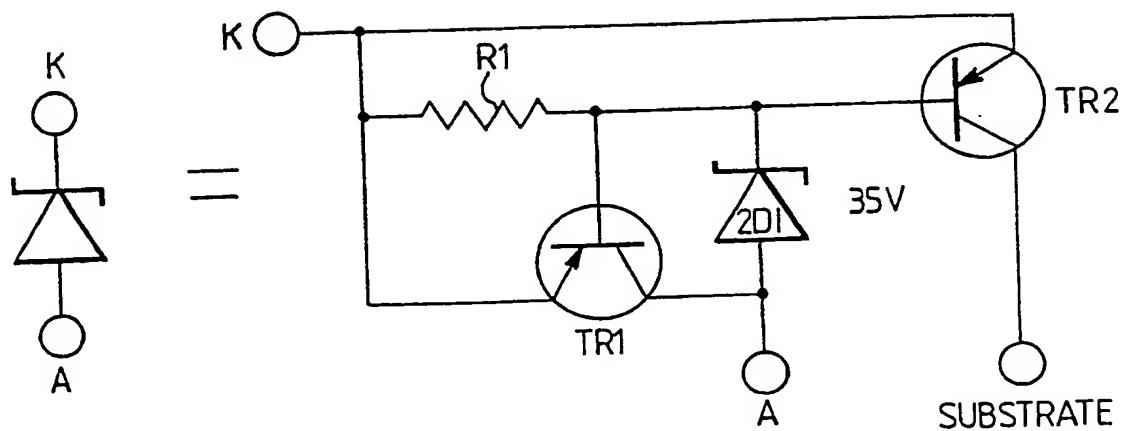


Fig.3

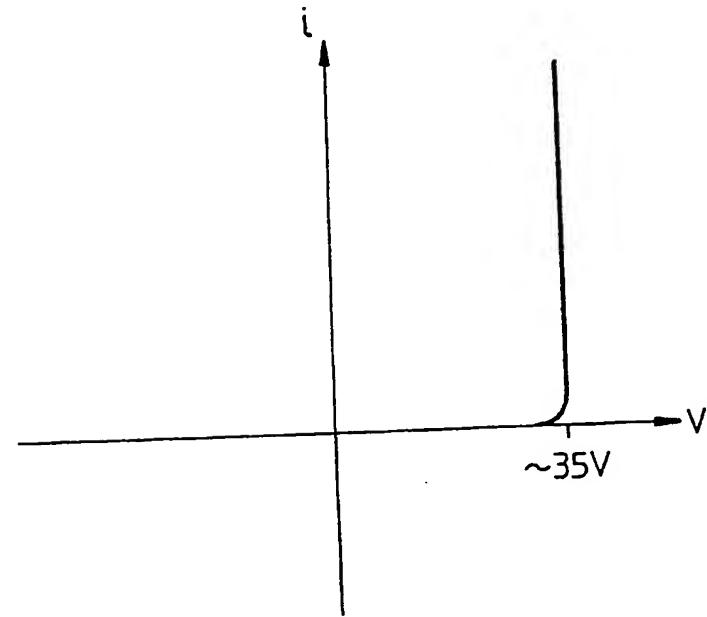


Fig.4

SPECIFICATION

Protection device for integrated circuits

- 5 This invention relates to overvoltage protection devices for integrated circuits, and in particular to an input protection arrangement for circuits fabricated by isolated bipolar techniques.
- 10 High density integrated circuits incorporating a large number of relatively small devices are subject to accidental voltage breakdown. Excess voltage can occur either as transients when the integrated circuit is in use, or as
- 15 static voltages applied to the circuit terminals when the circuit is handled prior to use. For example, the human body is often represented by a capacitance of 200pF and can easily be charged to a potential of 1 to 3 kilovolts. A
- 20 subsequent discharge through an integrated circuit can give rise to a transient current as high as a few amps. Even though a relatively small amount of energy is dissipated this is more than sufficient to damage the small and
- 25 delicate device structures in present day high density circuits.

A number of techniques have been proposed for overcoming this problem, each technique being adapted to the particular semiconductor process that is employed. In the case of integrated circuits of the isolated bipolar type, a number of protection techniques have been proposed.

- 30 For example diodes from an input to earth
- 35 and to supply can limit that terminal voltage to one diode drop above or below the supply of earth respectively. This method is undesirable as in certain circumstances the test discharge can increase the supply rail voltage
- 40 and thus allow too high a voltage on the input pin. Further devices utilise the breakdown characteristics of the base emitter or base collector junction of a transistor or an N+ emitter area diffused into P+ isolation. With
- 45 a high gain "Low Power Schottky" process capable of supporting I²L circuitry, the base collection junction exhibits too high a series resistance. The base emitter junction is too fragile due to the thin base involved and the
- 50 N+ diode into isolation has so "soft" a breakdown that it would load the input under normal operating conditions.

The object of the present invention is to overcome the aforementioned disadvantages.

- 55 According to the invention there is provided an overvoltage breakdown protection arrangement for a bipolar integrated circuit, the arrangement comprising first and second spaced p-type regions disposed in an n-type epitaxial
- 60 layer on a p-type substrate, an n-type region adjacent the second said p-type region, and a common connection between the n-type and second p-type regions.

With this arrangement both lateral and vertical PNP transistor action can occur to give a

low series resistance clamp to voltages in excess of the junction breakdown of the first p-type region diffused into the N-type epitaxial layer.

- 70 An embodiment of the invention will now be described with reference to the accompanying drawings in which:—

Figure 1 is a cross-sectional schematic view of the overvoltage protection arrangement;

- 75 Figure 2 is a plan view of the arrangement of Fig. 1;

Figure 3 shows the equivalent circuit of the protection arrangement of Figs. 1 and 2; and

- Figure 4 illustrates the typical breakdown

80 characteristics of the arrangement.

Referring to Figs. 1, 2 and 3, the protection arrangement, which typically forms part of an integrated bipolar circuit, is formed in an n-type epitaxial layer 11 disposed on a p-type

- 85 semiconductor substrate 12. The device which, in use is coupled between the circuit input terminals and earth, comprises first (13) and second (14) spaced p-type regions one of

- 90 region 15. A common connection is provided between the regions 14 and 15, which connection comprises the cathode terminal K of the arrangement. The anode terminal A of the arrangement is connected to the p-type region

- 95 13. The substrate 12 is normally connected to ground.

The arrangement can be regarded as two pnp transistors TR1 and TR2 (Fig. 4) the first

- 100 lateral transistor comprising the p-type region 14 (emitter) the n-type layer 11 (base) and p-type region 13 (collector) and the second vertical transistor comprising the p-type region 14 (emitter) the n-type layer 11 (base) and the p-type substrate 12 (collector). The pm junction between the region 13 and the layer 11

105 provides the equivalent Zener diode ZD1 of Fig. 3. Typically this junction has a breakdown voltage of about 35 volts. The resistor R1 of Fig. 3 is not a physical component but

- 110 represents the lateral spreading resistance in layer 11 of a section of the dotted path indicated in Fig. 1, between the layer contact in region 15 and point 16 under the edge of region 14 facing region 13.

- 115 When an excessive positive potential (e.g. greater than 35 volts) is applied to the cathode terminal with respect to the anode terminal, i.e. to the N-type layer 11 with respect to the P region 13, avalanche breakdown of this

- 120 junction occurs and the resultant cathode current (electrons) flows along the dotted paths indicated in Fig. 1, to reach the cathode terminal via the N+ contact region 15. The lateral voltage drop due to this current flowing

- 125 under region 14 to get to region 15 is of such a polarity to forward bias the region 14 junction to layer 11 above point 16 and allow a fraction of the original breakdown current to flow to the cathode terminal through this N/P junction. This latter fraction of the breakdown

- 130 130

2 current constitutes the emitter efficiency component of a base current for transistors TR1 and TR2 and allows a very much greater number of holes to be emitted from region 14 5 and collected by region 13 or the substrate 12. The resultant rapid increase in cathode current provides the low slope resistance in breakdown necessary to adequately clamp the large discharge current which can be encountered in protection networks. The structure is 10 also very robust due to the wide transistor base regions involved.

CLAIMS

- 15 1. An overvoltage breakdown protection arrangement for a bipolar integrated circuit, the arrangement comprising first and second spaced p-type regions disposed in an n-type epitaxial layer on a p-type substrate, an n-type 20 region adjacent the second said p-type region, and a common connection between the n-type and second p-type regions.
 2. An overvoltage breakdown protection arrangement for a bipolar integrated circuit, 25 including first and second p-type regions which together with an n-type layer therebetween form a lateral pnp transistor and an n-type region disposed adjacent the second p-type region and provided with a common 30 connection thereto, wherein the arrangement is such that an application of an overvoltage between n-type and the first p-type regions causes current flow past the second p-type region and the transistor thus providing a low 35 impedance discharge path.
3. An arrangement as claimed in claim 1 or 2, wherein means are provided for grounding the substrate whereby a further low impedance path comprising a vertical pnp transistor is provided.
- 40 4. An overvoltage breakdown protection arrangement substantially as described herein with reference to the accompanying drawings.
5. An integrated circuit provided with one 45 or more protection arrangements as claimed in claim 1, 2, 3 or 4.

